REMARKS

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority, and for indicating that the certified copy of the priority document, Japanese Patent Application No. Heisei 10-302893 dated October 23, 1998 has been made of record in the file.

Applicant requests that the Examiner consider the references listed on the Form PTO-1449 submitted with the Information Disclosure Statement filed on December 30, 1999 and initial same, thereby confirming that the listed references have been considered.

Applicant herein adds new claims 17-30. The new claims 17-30 are fully supported by the specification as originally filed, and add no new matter. An Excess Claims Fee Payment Letter is being concurrently filed with this Amendment. Entry and consideration of the above new claims is respectfully requested.

Applicant herein amends claims 3, 6 and 12 to remove grammatical errors and to remove awkward language. The amendments to claims 3, 6 and 12 do not narrow the literal scope of the claims, and are not made for reasons of patentability.

Claims 1-15 and 17-30 are all the claims presently pending in the application.

1. The Examiner indicates that Applicant is required to furnish drawings under 37 C.F.R. § 1.81. However, Applicant filed Formal Drawings when Application Serial No. 09/421,273 was filed on October 20, 1999 in the Patent Office. In order to expedite prosecution of this Application, Applicant filed a Submission of Formal Drawings on November 30, 2001 and a copy of the stamped filing receipt is attached hereto. Applicant respectfully requests that the Examiner acknowledge

receipt the Formal Drawings in the next Communication from the Patent Office and include the Form PTO-948 to indicate if the drawings are acceptable.

2. Claims 1-15 stand rejected under 35 U.S.C. § 101 because the claims allegedly improperly embrace or overlap two different statutory classes of invention. Applicant respectfully traverses the rejection of claims 1-15 for at least the reasons set forth below.

Applicant has editorially amended claims 1, 2, 4, 5, 7-11 and 13-15. No new matter has been incorporated as a result of the amendments to claims 1, 2, 4, 5, 7-11 and 13-15. Applicant has addressed the Examiner's concerns with regard to these claims, thus rendering the above rejection moot. Applicant hereby submits that the amendments to claims 1, 2, 4, 5, 7-11 and 13-15 were made merely to more accurately claim the present invention, and do not narrow the literal scope or spirit of the claims as originally filed.

The Examiner also indicates that a drawing of the device recited in claim 1 is required. Applicant respectfully submits that Figures 5, 11, 12, 13 and 14 depict the device recited in claim 1, and no additional drawings are necessary.

Thus, since there are no art-based rejections presently pending against claims 1-15, Applicant believes that claims 1-15 are now in condition for allowance. Applicant further believes that new claims 17-30 are in condition for allowance as well.

3. Claims 1-15 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Applicant respectfully traverses the rejection of claims 1-15 for at least the reasons set forth below.

Applicant has editorially amended claims 1, 2, 4, 5, 7-11 and 13-15. No new matter has been incorporated as a result of the amendments to claims 1, 2, 4, 5, 7-11 and 13-15. Applicant has addressed the Examiner's concerns with regard to these claims, thus rendering the above rejection moot. Applicant hereby submits that the amendments to claims 1, 2, 4, 5, 7-11 and 13-15 were made merely to more accurately claim the present invention, and do not narrow the literal scope or spirit of the claims as originally filed.

Thus, since there are no art-based rejections presently pending against claims 1-15, Applicant believes that claims 1-15 are now in condition for allowance. Applicant further believes that new claims 17-30 are in condition for allowance as well.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees necessary to maintain the pendency of this application, except for the Issue Fee, to our Deposit Account No. 19-4880.

Respectfully submitted,

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Date: February 21, 2002

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (*Amended*) A semiconductor integrated circuit device provided [fabricated] on a semiconductor substrate of one conductivity type, comprising:

shallow trench isolating regions having a first depth, and provided [formed] in surface portions of said semiconductor substrate for defining active areas therebetween [there-between];

a terminal provided [formed] on said semiconductor substrate[, and unavoidably applied with static charge];

a circuit component of an integrated circuit provided [formed] in one of said active areas, and connected between said terminal and a first source of constant voltage; and

a protection circuit provided [protecting said circuit component from said static charge, formed] in at least said one of said active areas, and comprising: [including]

a first impurity region of said one conductivity type provided [formed] under said at least one of said active areas, wherein said first impurity region is [and serving as] a base region of a bipolar transistor,

a second impurity region of the other conductivity type opposite to said one conductivity type provided [formed] in a surface portion of said first impurity region, connected to said terminal, wherein said second impurity region is [and serving as] one of an emitter region and a collector region of said bipolar transistor; and

a third impurity region of said other conductivity type connected to said first source of constant voltage, provided [formed] in another surface portion of said semiconductor substrate, wherein said third impurity region is [in such a manner that static charge flows through said first impurity region without substantial resistance due to said shallow trench isolating regions and serving as] the other of said emitter region and said collector region of said bipolar transistor.

2. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein [in which] said third impurity region further comprises: [has]

a first impurity sub-region provided [formed] in a surface portion of another active area adjacent to said one of said active areas; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

3. (*Amended*) The semiconductor integrated circuit device as set forth in claim 2, wherein [in which] said first impurity sub-region comprises: [has]

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

4. (*Amended*) The semiconductor integrated circuit device as set forth in claim 2, wherein [in which] said circuit component is a field effect transistor comprising [having] source and drain

regions of said other conductivity type provided [formed] in said one of said active areas, and one of said source and drain regions is [serves as] said second impurity region.

5. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein [in which] said third impurity region comprises: [has]

a first impurity sub-region provided [formed] in another surface portion of said first impurity region spaced from said second impurity region; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

6. (*Amended*) The semiconductor integrated circuit device as set forth in claim 5, wherein [in which] said first impurity sub-region comprises: [has]

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

7. (*Amended*) The semiconductor integrated circuit device as set forth in claim 5, wherein [in which] said circuit component is a field effect transistor comprising [having] source and drain regions of said other conductivity type provided [formed] in said one of said active areas, wherein one of said source and drain regions is [serves as] said second impurity region, and the other of said source and drain regions is [serves as] said first impurity sub-region.

8. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein [in which] said third impurity region is provided [formed] in another active area adjacent to said one of said active areas and having a second depth greater than said first depth.

9. (*Amended*) The semiconductor integrated circuit device as set forth in claim 8, wherein [in which] said circuit component is a field effect transistor comprising [having] source and drain regions of said other conductivity type provided [formed] in said one of said active areas, and one of said source and drain regions is [serves as] said second impurity region.

10. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein [in which] said third impurity region is provided [formed] in another surface portion of said first impurity region and deeper than said second impurity region.

11. (*Amended*) The semiconductor integrated circuit device as set forth in claim 10, wherein [in which] said circuit component is a field effect transistor comprising [having] source and drain regions of said other conductivity type provided [formed] in said one of said active areas, one of said source and drain regions is [serves as] said second impurity region, and the other of said source and drain region is [serves as] a part of said third impurity region.

12. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein [in which] said third impurity region extends in said first impurity region under said second impurity region.

13. (*Amended*) The semiconductor integrated circuit device as set forth in claim 10, wherein [in which] said circuit component is a field effect transistor comprising [having] source and drain regions of said other conductivity type provided [formed] in said one of said active areas, and one of said source and drain regions is [serves as] said second impurity region.

14. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein [in which] said terminal is [serves as] a signal output terminal, and said circuit component is an output transistor.

15. (*Amended*) The semiconductor integrated circuit device as set forth in claim 1, wherein [in which] said terminal is [serves as] a signal input and output terminal, and said circuit component is an output transistor comprising a portion [forming a part] of an input and output circuit connected to said terminal.

Claims 17-30 are added as new claims.